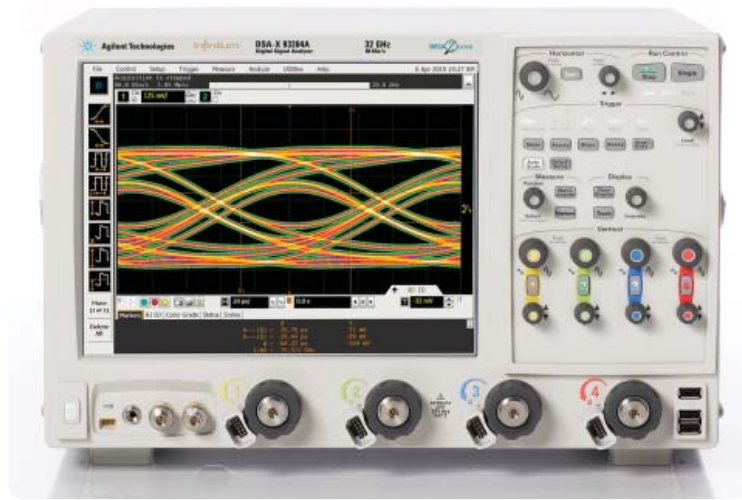


PCI Express® Transmitter Electrical Validation and Compliance Testing with Agilent Infiniium Oscilloscopes

Application Note 1496



Who should read this application note?

This application note is intended for digital designers and developers validating electrical performance of PCI Express®-based designs and working toward electrical compliance of PCI Express products.

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Agilent Technologies

Introduction

The PCI bus is the de-facto standard I/O bus for connecting devices inside a personal computer. As speed demands for I/O have increased, the PCI bus has reached its limits. The synchronously clocked architecture of PCI limits its speed due to difficulty in controlling data to clock skew. The parallel nature of the PCI data bus makes circuit-board layout difficult when you are trying to match delays among data lines. The fastest version of parallel-type PCI is PCI Express 3.0 which can reach 25.6 GBytes/s of bandwidth.

PCI Express overcomes the speed limits by replacing PCI's synchronously clocked and multi-drop parallel bus with multiple embedded-clock serial links running at 8 GT/s. Each serial link transfers data in one direction only, and it can be routed as a differential trace pair relatively independent of the other links. This architecture greatly simplifies board layout. A pair of links, called a "lane," moves data in opposite directions between two devices. Validating PCI Express performance involves characterizing the reference clock and data signals. Your product must successfully pass "Gold Suite" testing – a superset of what the PCI-SIG® SigTest tests – at a PCI-SIG workshop using the official PCI-SIG approved test fixtures. Key parameters are rise-time, amplitude, eye width, jitter and Phase-Locked Loop (PLL) bandwidth and peaking. For more information, visit the official PCI-SIG Web site at www.pcisig.com.

Whether you are troubleshooting, capturing contiguous waveforms, ensuring correct operation, or proving compliance, an oscilloscope with low noise, low jitter, and high probe accuracy is critical for measurement accuracy. The Agilent 90000 Series real time oscilloscope and the Agilent 86100 Infiniium DCA have the capabilities you need for these measurements. This application note provides an overview of how to use these Infiniium oscilloscopes for PCI Express validation and compliance testing.

PCI Express basic specifications

Table 1 lists the basic electrical specifications for PCI Express transmitters. Detailed specifications for PCI Express transmitter and receiver ICs can be found in the PCI Express Base Specification Revision 3.0, available from the PCI-SIG Web site. For detailed specifications on the 100-MHz reference clock and the system (motherboard) adapter card connector interface, see the PCI Express Card Electromechanical Specification Revision 3.0.

Table 1. PCI Express transmitter basic specifications

PCI Express version	1.0a	1.1	2.0	3.0
Specification released	2003	2005	2007	2010
Data transfer rate	2.5 GT/s	2.5 GT/s	5.0 GT/s	8.0 GT/s
Data fundamental frequency	1.25 GHz	1.25 GHz	2.5 GHz	4.0 GHz
Data encoding	8b/10b	8b/10b	8b/10b	PRBS23 Scrambling
Total bandwidth for x16 link	~6.4 GB/s	~6.4 GB/s	~12.8 GB/s	~25.6 GB/s
Key changes	Initial release	Tighter jitter and reference clock tests	Speed, Cable specification, PLL bandwidth test, tighter jitter and reference clock tests, new de-emphasis levels	Speed, higher PLL bandwidth, more complex de-emphasis, scrambling, others still being decided

Silicon validation

New and existing silicon ICs with PCI Express ports on them must be validated. Silicon vendors will need to show customers that their ICs meet the PCI Express specifications. OEMs purchasing these ICs may wish to audit the ICs' electrical performance before incorporating them into their products.

There are two main areas of silicon validation: transmitter testing, and receiver testing. This application note focuses on transmitter testing. Receiver testing is discussed in a separate application note, *Accurate Calibration of Receiver Stress Test Signals for PCI Express® rev. 3.0 Assuring Interoperability at Data Rates of 8 GT/s* (publication number 5990-6599EN).

If you want to validate all PCI Express specifications, you will need a real-time oscilloscope with the N5393C PCI Express Electrical Performance Validation and Compliance Software and the E2688A high speed serial data analysis (SDA) software. N5465A InfiniiSim Waveform Transformation Toolset is recommended. Table 2 shows PCI Express 1.0, 2.0, and 3.0 data rates and their recommended oscilloscopes and bandwidth.

It is important to calibrate out skew between the cables connecting the transmitter to the oscilloscope and to use high-quality cables of the shortest possible length to minimize high-frequency cable loss. Deskeewing the cables allows you to use the oscilloscope's built-in math functions and measurements to validate the true differential signal and analyze the common-mode voltage of the lane(s) under test.

Table 2. Tested data rates and recommended oscilloscopes

Data rate	Recommended oscilloscope	Bandwidth of recommended oscilloscope
2.5 Gb/s	DSO/DSAX91604A	16 GHz
	DSO/DSAX92004A	20 GHz
	DSO/DSAX92504A	25 GHz
	DSO/DSAX92804A	28 GHz
	DSO/DSAX93204A	32 GHz
	DSO91304A	13 GHz
	DSO91204A	12 GHz
	DSO90804A	8 GHz
	DSO90604A	6 GHz
5.0 Gb/s	DSO/DSAX91604A	16 GHz
	DSO/DSAX92004A	20 GHz
	DSO/DSAX92504A	25 GHz
	DSO/DSAX92804A	28 GHz
	DSO/DSAX93204A	32 GHz
	DSO91304A*	13 GHz
	DSO91204A	12 GHz
8.0 Gb/s	DSO/DSAX91604A	16 GHz
	DSO/DSAX92004A	20 GHz
	DSO/DSAX92504A	25 GHz
	DSO/DSAX92804A	28 GHz
	DSO/DSAX93204A	32 GHz
	DSO91304A*	13 GHz
	DSO91204A	12 GHz

* DSA model equivalents are also compatible

Serial data analysis

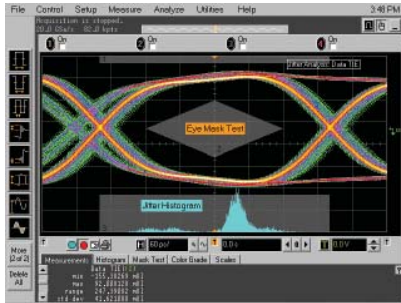


Figure 1. PCI Express eye and jitter measurement using E2688A SDA software with SigTest DLL

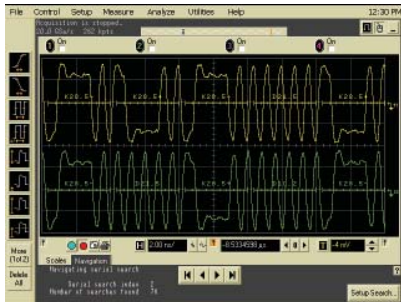


Figure 2. Lane-lane deskew and packet decode using E2688A SDA software with SigTest DLL

2. More information about SigTest measurement techniques can be found at www.pcisig.com
3. The compliance pattern consists of four symbols, K28.5-, D21.5, K28.5+, D10.2, which repeats continuously on each lane, except when the delay characters are inserted. The delay characters are simply K28.5 comma symbols and are inserted two before and two after the compliance pattern once every 640 UI (8 symbols times 8 lanes times 10 UI per symbol). The polarity of the K28.5 comma symbols used as delay characters is adjusted to satisfy the running disparity on the bus, such that the two delay characters preceding the compliance pattern will be K28.5- and K28.5+, respectively. The same is true for the two delay characters following the compliance pattern.

Agilent's E2688A high-speed serial data analysis (SDA) software for the real-time oscilloscopes provides PCI Express-specified clock recovery, real-time eye diagram, and jitter measurements. For PCI Express Base Specification 1.0a, the E2688A high-speed SDA software incorporates the PCI-SIG SigTest DLL to perform these measurements, ensuring consistent results with PCI-SIG workshop compliance testing, which also uses SigTest. The SigTest DLL recovers a clock over an analysis window of 3500 unit intervals (UIs). Then 250 consecutive UIs located in the middle of this analysis window are overlaid to display the eye diagram and measure the jitter². The 3500 UI clock recovery window (CRW) is then advanced 100 UIs from its previous starting point, and the jitter measurement is repeated. Using this method, 215 individual jitter measurements are taken over a 25,000 UI compliance pattern length to give a composite estimate of total jitter and signal eye-diagram quality. Figure 1 shows an example of using the E2688A high-speed serial data analysis tool and the PCI-SIG SigTest DLL to perform a transition-bit eye and jitter measurement.

SDA as debugging tool

Additionally, for PCIe[®] 1.x and 2.x, the serial data analysis packages is a powerful debug tool and is enabled with 8b/10b symbol decode of the serial bit-stream to allow quick insight into packet decode and lane-to-lane symbol alignment. Figure 2 shows the full 8b/10b decode of transmitter Lane 0 and Lane 1 on a PCI-Express x8 link. The compliance pattern is implemented with delay characters before and after the compliance pattern to create worst-case crosstalk on adjacent lanes. The delay characters are advanced to each successive lane and the process repeated for each set of eight lanes in a link, such that the delay characters will only be transmitted on any given lane once every 640 UI³, or every 256 ns.

You can also use the mask test feature to identify the specific digital patterns that caused a specific failure in the eye diagram when testing under the 1.1 specification (using a first order PLL). For 2.0 testing you can use a first or second order PLL for clock recovery and apply a TIE brick wall filter (included with the E2688A Series Data Analysis package) to achieve a proper clock filtering. Figure 3 shows how to trigger on a mask failure and unfold the eye to find the failing bit. (3.0 eye and jitter will be discussed in detail in the following sections)

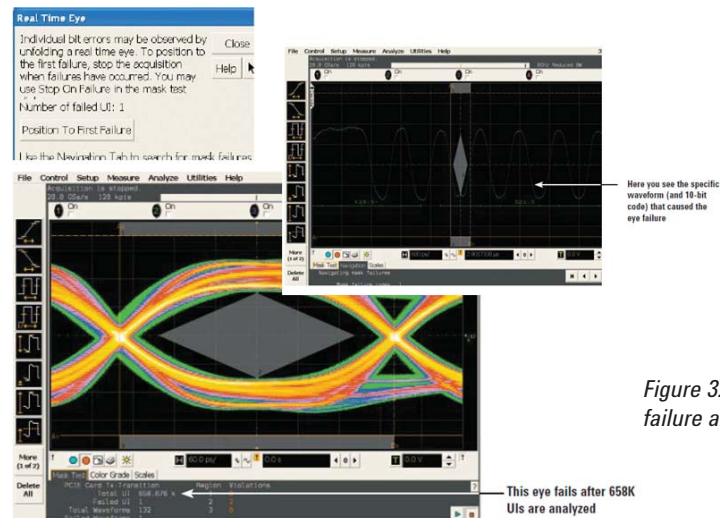


Figure 3. Eye diagram failure analysis

InfiiSim Waveform Transformation Toolset

N4565A InfiiSim Waveform Transformation Toolset for de-embedding of test fixtures. Introduced with PCIe 2.0, de-embedding of test fixtures utilizes S-parameters as input to create a de-embed model that helps to restore high frequency signal content that is often lost or significantly attenuated by test fixtures and cables. This can help to recover significant jitter margin normally lost to fixtures used in a test setup.

S-parameters can be entered into InfiiSim in various block diagrams (see Figure 4) that represent the measurement setup to create a transfer function. The transfer function is used to derive a time domain 'filter' that is convolved with the acquisition to transform the acquired waveform to a waveform at the desired measurement location. See the application note *The ABC's of De-Embedding* (publication number 5989-5765EN).

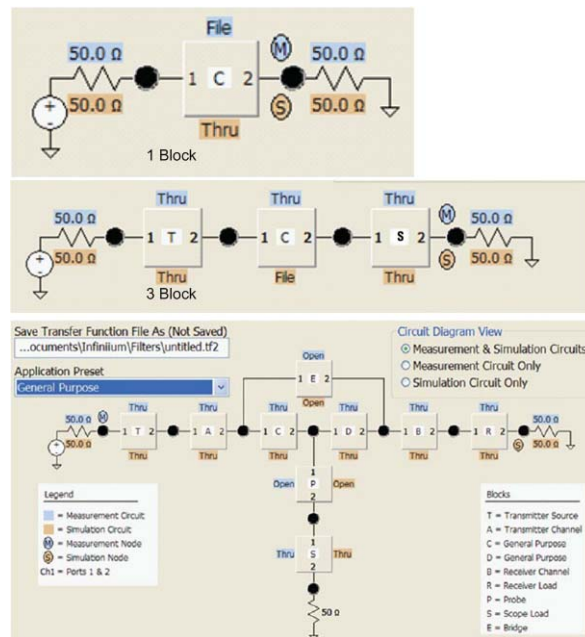


Figure 4. InfiiSim can model a simple channel to a sophisticated system

Compliance testing

Compliance testing is performed at PCI-SIG workshops on systems (motherboards) and add-in adapter cards. Passing the compliance tests is a requirement for vendors to be included on the PCI-SIG integrators list and to use the PCI Express logo. The Agilent 90000 Series oscilloscopes are approved by the PCI-SIG for compliance testing. Figure 5 shows the Infiniium oscilloscope being used by PCI-SIG testers at the workshop to support PCI Express testing. In addition, compliance testing also requires test fixtures and the PCI-SIG SigTest software. Detailed test procedures are available from www.pcisig.com.

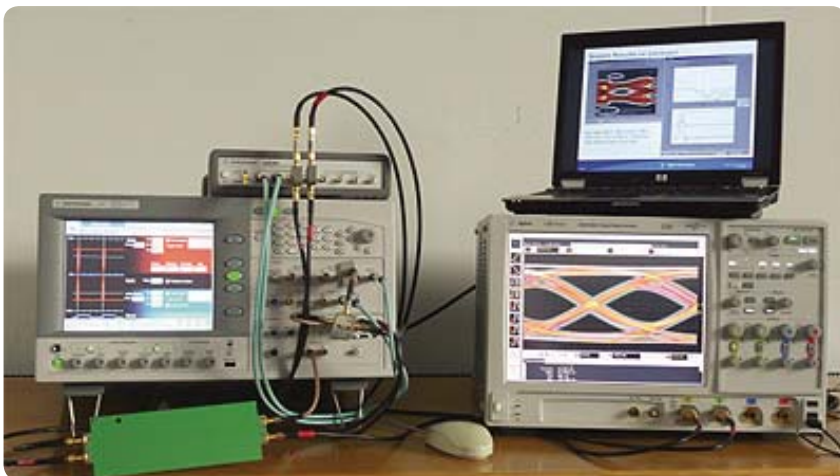


Figure 5. Agilent Infiniium oscilloscope in use at PCI-SIG Workshop

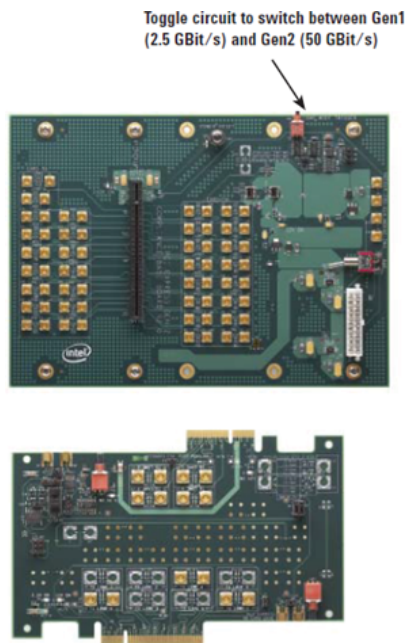


Figure 6. The PCI-SIG Compliance Base Board (CBB2) for Gen2 add-in card testing, and the Compliance Load Board (CLB2) for Gen2 motherboard or host system testing.

Two test fixtures can be used for compliance testing. Figure 6 shows the compliance base board for Gen2 (CBB2), which is used for testing add-in adapter cards. The CBB supports testing adapter cards up to 16 lanes. The lanes of the adapter card's TX outputs can be connected directly to the scope inputs. The lanes can also be measured with a differential probe, such as the Agilent 1169A 12-GHz InfiniiMaxII differential active probe. A 100-MHz reference clock oscillator is contained on the CBB to provide the system clock for add-in adapter card testing, or an external reference clock can be provided by the add-in adapter card under test.

Figure 6 also shows the compliance load board for Gen2 (CLB2) used for testing systems (motherboards). The CLB has edge connectors on four sides to support testing of 1-, 4-, 8-, and 16-lane system connectors. As with the CBB, you can connect it to the scope using either SMA cables or differential active voltage probes.

To purchase the PCI Express compliance test fixtures, consult the PCI-SIG Web site and select the PCI-SIG specification order form link at: www.pcisig.com/specifications/ordering_information. Currently, PCI-SIG does not offer fixtures for the 3.0 specification, consult the PCI-SIG Web site for updates.

Compliance testing (continued)

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1169A (for 2.0 5 GT/s and 3.0 or 1134A for 1.x and 2.0 2.5 GT/s) probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s (for 2.0 5 GT/s and 3.0 or 20 GS/s for 1.x and 2.0 2.5 GT/s) sample rate available on two channels.
- Use one differential probe head with the 1169A (for 2.0 5 GT/s and 3.0 or 1134A for 1.x and 2.0 2.5 GT/s) probe amplifier and the Ch2 input of an oscilloscope that has 40 GS/s (for 2.0 5 GT/s and 3.0 or 20 GS/s for 1.x and 2.0 2.5 GT/s) sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the compliance patter defined in the base specification (1.x, 2.x, or 3.x) will be transmitted. Figure 7 shows these three probing options.

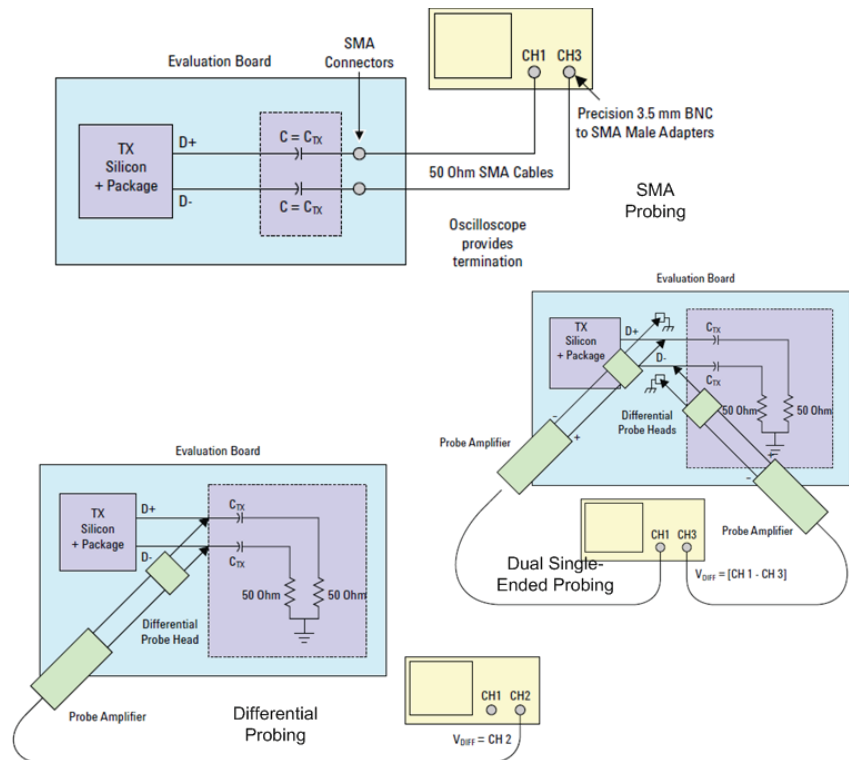


Figure 7.

Signal quality testing

When you connect a PCI Express transmitter link to the specified passive termination network, such as the CBB or CLB fixture, the device should start generating the compliance test pattern shown in Figure 1 on its TX output lanes⁴. You can use your oscilloscope to save this compliance signal as XY pairs in a comma-separated-value (CSV) formatted file. Then you can use SigTest software to read this CSV file and perform signal quality tests on the compliance pattern. The software tabulates and displays the pass/fail results, as shown in Figure 8. SigTest software tests the data rate, unit interval, jitter, and eye diagrams for both transition and non-transition bits. Failing items are identified with red indicators.

SigTest software also generates a summary test report in HTML format as shown in Figure 9, which shows overall pass/fail, data rate, jitter, and eye diagrams. You can use the SigTest application conveniently on the oscilloscope's open Windows[®] XP operating system. If you wish, you can use a secondary display monitor to extend the Windows desktop so that SigTest does not have to run in the oscilloscope signal viewing area. SigTest software is available from www.pcisig.com.

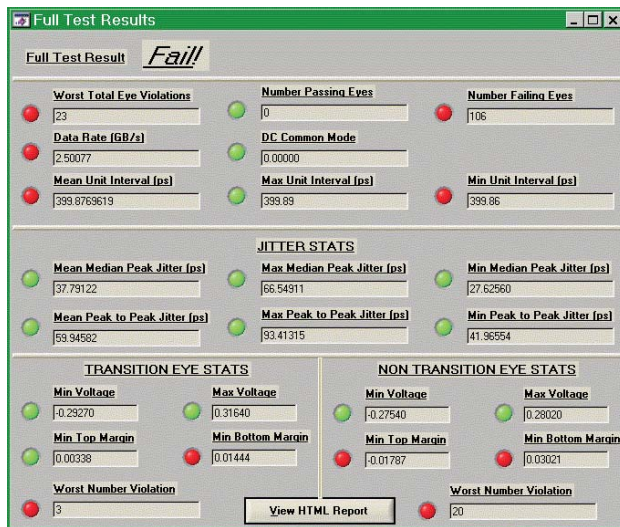


Figure 8. SigTest software test-result status screen

- The transmitter attempts to detect a receiver on all lanes of a possible link. Once a far-end termination is determined to be present, the Link Training and Status State Machine (LTSSM) will enter the Polling.Compliance state and begin transmitting the compliance pattern on all lanes with a detected receiver termination until an electrical idle has been detected at the receiver.

Test Results for PCIe_test_data+

Required Tests:

- Overall Result: **Fail!**
- Data Rate: 2.500678 GB/s
Data Rate Pass!
- Median to Peak Jitter: 66.549108 ps
Median to Peak Jitter Pass!
- Peak to Peak Jitter: 93.41315 ps
Peak to Peak Jitter Pass!
- Eye Violations: 23 points
Eye Test Fail!

Worst Non Transition Signal Eye

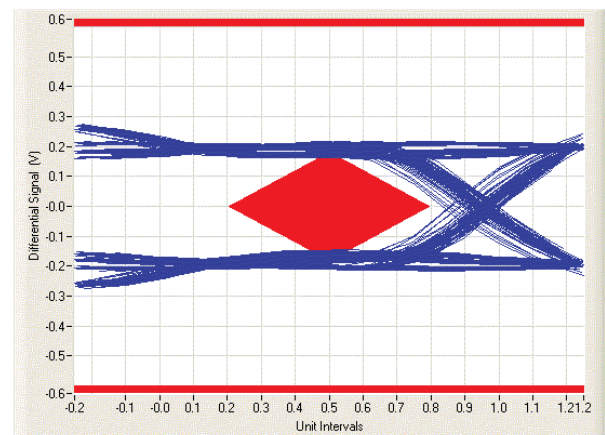


Figure 9. SigTest HTML test report

Automated electrical compliance testing

In addition to passing the SigTest signal quality tests at the compliance workshop events, the PCI-SIG requires that PCI Express systems and add-in adapter cards pass a rigorous suite of electrical transmitter compliance tests. You must perform these tests before you attend the compliance workshop events. These tests are published on www.pcisig.com and are available as test assertions in the PCI Express Base Specification for 1.x, 2.x, and 3.x. The difficulty in implementing many of these tests is the instrumentation setup and probe calibration time required to properly capture, analyze and display the pass/fail results of these tests with respect to the limits specified.

The Agilent N5393C PCI Express Electrical Performance Validation and Compliance software automates all of the tests required for full compliance and margin testing and provides a customized test-setup walkthrough for each test to ensure proper electrical termination and connection to the device under test, whether it be at the interface on the CLB/CBB for final device compliance and interoperability testing or at the silicon package pins during early turn-on validation.

The previous sections discuss serial data analysis (clock recovery, eye measurements, and jitter), InfiniiSim (de-embedding), SigTest DLLs required for test, fixtures, and probing options. The N5393C software integrates and automates all these things to test all PCI Express 1.x, 2.x, and 3.x specifications.

There are different compliance patterns and clock recovery methods required for each generation of PCI express. Earlier in this application note, we described the 1.0a clock recovery algorithm that is integrated into the serial data analysis tool. For PCI Express 3.0, for unit interval and jitter measurements, the compliance pattern requires 64 ones and 64 zeroes pattern. The N5393C software automatically calls and runs a MATLAB function (DPSerialEye) to generate a clock recovery for the 64-ones/64-zeroes segment to create an impulse signal for each segment. The real time eye can then be folded using this impulse pattern and measurements made and reported. Based on base specification selection in the application, the N5393C software selects and runs to appropriate clock recovery, SigTest DLL, and reports the results compared to their respective specifications. Figure 10 shows the final html report that the N5393C generates with the same SigTest output as SigTest provides, but with additional information of test setup, and margin analysis.

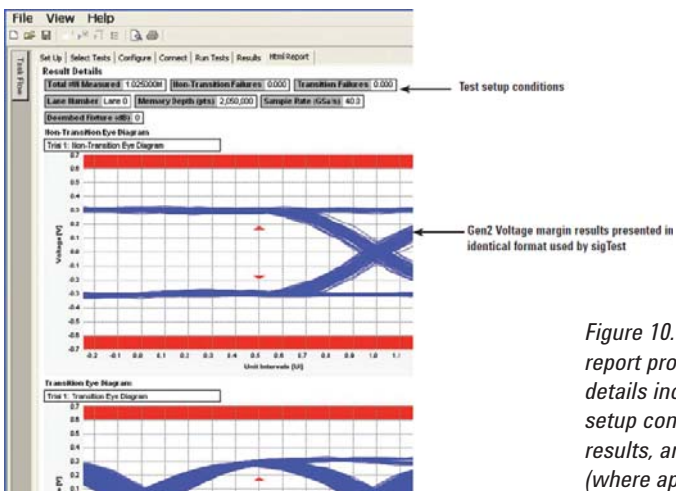


Figure 10. The HTML report provides additional details including test setup conditions, graphical results, and test limits (where appropriate)

Automated electrical compliance testing (continued)

The N5393C software also integrates the InfiniiSim de-embedding into the measurements made. Figure 11 shows the selection screen where you can load your transfer function, select the best bandwidth limiting for your measurement, and any response correction.

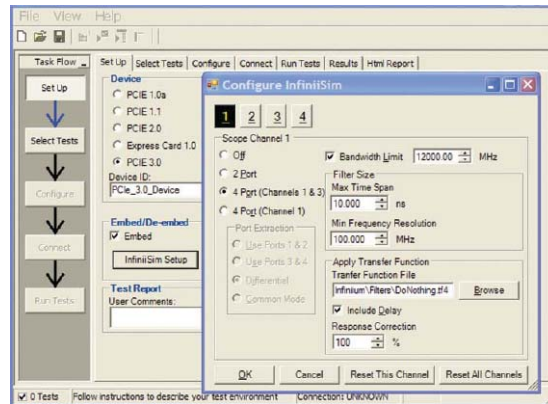


Figure 11 The N5393C integrates de-embedding capability when coupled with the optional N5465A InfiniiSim waveform transformation toolset

Finally, the N5393C automates test selection, probing setup choices, and provides a step by step connection setup to meet your test and probing selections. Ultimately, reducing error and confusion in the complex PCI Express measurements.

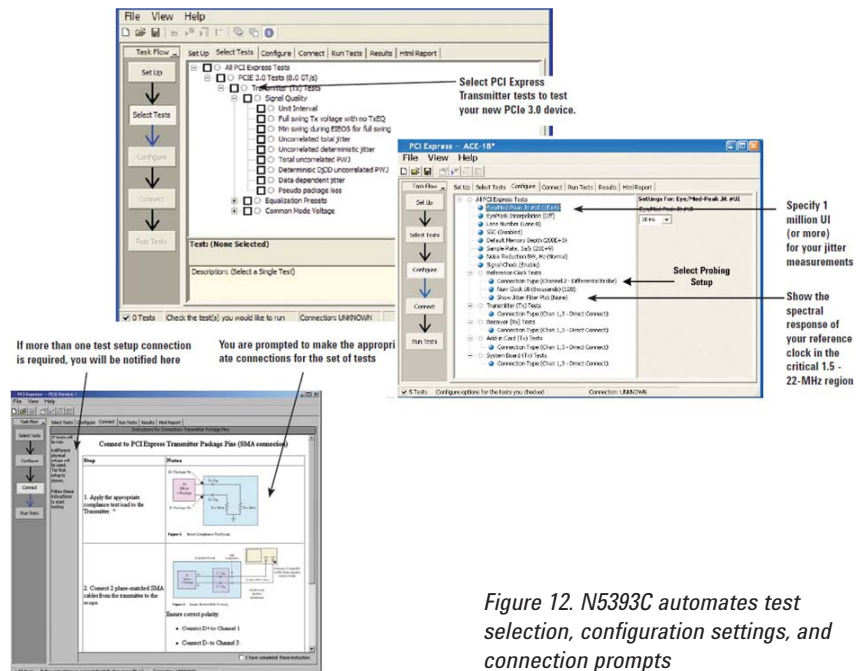


Figure 12. N5393C automates test selection, configuration settings, and connection prompts

Summary

PCI Express uses completely different clocking and data transmission schemes compared to its parallel-PCI-bus predecessors. It is no longer crucial to have length-matched traces from one lane to the next, nor a synchronous clock distributed between adjacent devices. However, the switch to serially transmitted data at higher bit rates has brought with it the need for more complex clock recovery and jitter measurement techniques to allow you to view the transmit data as it would be seen by the receiver PLL and analyze its signal fidelity. As with any standard, PCI Express transmitter compliance testing requirements may continue to evolve over time. This application note should continue to provide a solid foundation for understanding the compliance testing requirements as set forth by the PCI Express Base Specification Revision 1.0a.

Glossary

DCA Digital communication analyzer
SDA Serial data analysis
PCIe PCI Express
PCI-SIG Peripheral Component Interconnect Special Interest Group

Related Literature

Publication title	Pub number
<i>Agilent Technologies N5393C PCI Express® 3.0 (Gen3) Electrical Performance Validation and Compliance Software for Infiniium Oscilloscopes Data Sheet</i>	5989-1240EN
<i>Accurate Calibration of Receiver Stress Test Signals for PCI Express® rev. 3.0 Assuring Interoperability at Data Rates of 8 GT/s Application Note</i>	5990-6599EN
<i>Agilent Technologies E2688A, N5384A High-Speed Serial Data Analysis and Clock Recovery Software for Infiniium Oscilloscopes Data Sheet</i>	5989-0108EN
<i>Understanding Oscilloscope Frequency Response and Its Effect on Rise-Time Accuracy Application Note 1420</i>	5988-8008EN
<i>Agilent N5393A PCI Express Automated Test Application 1.0a Product Manual</i>	N5393-97000
<i>Agilent Technologies N5465A: InfiniiSim Waveform Transformation Toolset for the Infiniium Series Oscilloscopes Data Sheet</i>	5990-4059EN

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